CLAIMS

What is claimed is:

1. A method for forming a metallic silicide film and dielectric cap during a gate stack formation wherein said gate stack includes a polysilicon layer, comprising:

forming said metallic silicide film in a non-annealed state over said polysilicon layer; and

forming said dielectric cap on said metallic silicide film at sufficiently low temperature that said metallic silicide film remains in said non-annealed state.

2. The method of claim 1 wherein forming said dielectric cap occurs at a temperature below about 600°C.

3. A method for forming a gate stack, comprising:

providing a semiconductor substrate with a dielectric layer on an active surface of said semiconductor substrate, wherein a polysilicon layer is disposed over said dielectric layer;

forming a metallic silicide film in a non-annealed state over said polysilicon layer;

forming a dielectric cap on said metallic silicide film at a sufficiently low temperature that said metallic silicide film remains in said non-annealed state;

forming and patterning a resist layer on said dielectric cap;

etching said dielectric cap, said metallic silicide film, and said polysilicon layer; and

stripping said resist layer.

4. The method of claim 3 wherein forming said dielectric cap occurs at a temperature below about 600°C.

5. In a method of forming a gate stack wherein a layered structure is fabricated by forming a dielectric layer on an active surface of a semiconductor

substrate, forming a polysilicon layer on said dielectric layer, forming a metallic silicide film on said polysilicon layer, forming a dielectric cap on said metallic silicide film, forming and patterning a resist layer on said dielectric cap, etching said layered structure, an stripping said resist layer, the improvement comprising:

forming a metallic silicide film in a non-annealed state over said polysilicon layer; and

forming a dielectric cap on said metallic silicide film at sufficiently low temperature that said metallic silicide film remains in said non-annealed state.

6. The method of claim 5 wherein forming said dielectric cap occurs at a temperature below about 600°C.

7. A method for forming a gate stack, comprising the steps of:

forming a layered structure, comprising the steps of:

providing a semiconductor substrate having a dielectric layer on an active surface thereof with a polysilicon layer disposed over said dielectric layer,

forming a metallic silicide film over said polysilicon layer, and

forming a dielectric cap on said metallic silicide film;

subjecting at least said metallic silicide film of said layered structure to at least one heat cycle during said forming of said layered structure;

implanting said layered structure;

forming and patterning a resist layer on said dielectric cap;

etching said dielectric cap, said metallic silicide film, and said polysilicon layer; and

stripping said resist layer.

8. The method of claim 7, wherein implanting said layered structure comprises ion implantation.

9. The method of claim 8, wherein said ion implantation comprises implantation of ions selected from the group consisting of silicon, tungsten, and argon.

10. The method of claim 7, wherein implanting said layer structure comprises doping.

11. The method of claim 10, wherein said doping comprises doping with a dopant selected from the group consisting of phosphorous, arsenic, and boron.

12. The method of claim 7, wherein said at least one heat cycle occurs after said formation of said metallic silicide film on said polysilicon layer to anneal said metallic silicide film.

13. The method of claim 7, wherein said at least one heat cycle occurs during said formation of said dielectric cap on said metallic silicide film.

14. The method of claim 7, wherein said at least one heat cycle includes a temperature of at least 600°C.

15. In a method of forming a gate stack wherein a layered structure is fabricated by forming a dielectric layer on an active surface of a semiconductor substrate, forming a polysilicon layer on said dielectric layer, forming a metallic silicide film on said polysilicon layer, forming a dielectric cap on said metallic silicide film, subjecting at least said metallic silicide film of said layered structure to at least one heat cycle resulting in the formation of undesired silicon clusters within said metallic silicide film, forming and patterning a resist layer on said dielectric cap, etching said layered structure, and stripping said resist layer, the improvement

comprising implanting said layered structure to disperse said undesired silicon clusters prior to etching said layered structure.

16. The method of claim 15, wherein implanting said layer structure comprises ion implantation.

17. The method of claim 16, wherein said ion implantation comprises implantation of ions selected from the group consisting of silicon, tungsten, and argon.

18. The method of claim 15, wherein implanting said layer structure comprises doping.

19. The method of claim 18, wherein said doping comprises doping with a dopant selected from the group consisting of phosphorous, arsenic, and boron.

20. The method of claim 15, wherein said at least one heat cycle occurs after said formation of said metallic silicide film on said polysilicon layer to anneal said metallic silicide film.

21. The method of claim 15, wherein said at least one heat cycle occurs during said formation of said dielectric cap on said metallic silicide film.

22. The method of claim 15, wherein said at least one heat cycle includes a temperature of at least 600°C.

23. A gate stack, including a metallic silicide film in a non-annealed state.

24. A gate stack, including a metallic silicide film in an annealed state wherein said metallic silicide is substantially devoid of silicon clusters.

25. A gate stack on a dielectric layered semiconductor substrate, comprising:

a polysilicon layer disposed over said dielectric layered semiconductor substrate;

a metallic silicide film in a non-annealed state disposed over said polysilicon layer; and

a dielectric cap on said metallic silicide film formed at a sufficiently low temperature that said metallic silicide film remains in said non-annealed state.

26. A gate stack structure comprising a gate stack on a dielectric layered ~~semiconductor substrate wherein said dielectric layer is substantially devoid of pitting.~~

27. The gate stack structure of claim 26 wherein said a gate stack includes a non-annealed metallic silicide film.

28. The gate stack structure of claim 26 wherein said a gate stack includes an annealed metallic silicide film.